IN THE DRAWINGS

Corrected drawings are supplied herewith.

Enclosed are Replacement Sheets showing the following amendment to figures 1-5.

Figure 1 has been amended to denote the figure as prior art.

Figure 2 has been amended to correctly denote the A11,10,9 of address signal 230 as a row address RA instead of as a bank address BA. Applicant respectfully submits that support for the amendment to figure 2 is found in the specification, including the A11,10,9 description of original figure 2, and original figure 4.

Figure 3 has been amended to correctly denote the A12(NC),11,10,9,8 of address signal 330 as a row address RA instead of as a bank address BA. Applicant respectfully submits that support for the amendment to figure 3 is found in the specification, including at page 6, line 14, the A12(NC),11,10,9,8 description of original figure 3, and original figure 4.

Figure 4 has been amended to correctly denote the A2,1,0 of address signal 430 as a row address RA instead of as a bank address BA. Applicant respectfully submits that support for the amendment to figure 4 is found in the specification, including the A2,1,0 description of original figure 4, and original figure 2.

Figure 5 has been amended to correctly denote the A12(NC),11,10,9,8 of address signal 530 as a row address RA instead of as a bank address BA. Applicant respectfully submits that support for the amendment to figure 5 is found in the specification, including at page 7, lines 9-10, the A12(NC),11,10,9,8 description of original figure 5, and original figure 4.

Accordingly, Applicant respectfully submits that these changes do not introduce new matter. Applicant respectfully requests entry of amended drawings.

REMARKS

Claims 1-3, 5-6, 8-16, 18-21, 23-28, 30, 32-34, 36 and 38 are amended, no claims are canceled, and claims 39-79 are added; as a result, claims 1-34 and 36-79 are now pending in this application.

Applicant herein lists claim 35 as canceled. Applicant notes that the application was filed without a claim 35.

Applicant has amended claims 10, 14, 26, 32 and 34 to correct minor typographical errors. Applicant notes that such amendments were made to correct the minor typographical errors, and not in response to a prior art rejection of the claims.

Applicant has amended claims 1, 3, 5, 8-9, 11-12, 15, 18, 21, 24, 28, 32 and 36 to more particularly point out and distinctly claim certain aspects of the present subject matter. Applicant respectfully submits that such amendments are fully supported by various portions of the specification, including the summary, the abstract, the description at page 8, lines 12-14, and figures 2-6.

Accordingly, Applicant submits that no new matter has been introduced, and respectfully requests entry of the amendments to claims.

Applicant is presenting new claims 39-48 to incorporate the amended subject matter of objected to claims 2, 6, 10, 14, 16, 19, 23, 27, 30 and 33. Applicant respectfully submits that such new claims are fully supported by various portions of the specification, including originally-filed claims 2, 6, 10, 14, 16, 19, 23, 27, 30 and 33 respectively.

Applicant is presenting new claims 49-79 to more particularly point out and distinctly claim certain aspects of the present subject matter.

Applicant is presenting new claim 49. Applicant respectfully submits that such new claim 49 is fully supported by various portions of the specification, including the description, originally-filed claims 1, 5, 8, 11, 15, 18, 21, 24, 28, 32 and 36, and figures 2-6.

Applicant is presenting new claims 77-79. Applicant respectfully submits that such new claims 77-79 are fully supported by various portions of the specification, including the description, the originally filed claims, and figures 2-6.

Applicant is presenting new claims 50-57 and 69-76. Applicant respectfully submits that such new claims are fully supported by various portions of the specification, including the description, originally-filed claims 1, 5, 7-9, 11-12, 15, 18, 21, 24-26, 28, 31-32, 43, 36 and 38, and figures 2-6.

Applicant is presenting new claims 58 and 61-62. Applicant respectfully submits that such new claims are fully supported by various portions of the specification, including the description, originally-filed claims 1, 5, 8, 11, 15, 18, 21 and 24, and figures 2-5.

Applicant is presenting new claims 59 and 63-64. Applicant respectfully submits that such new claims are fully supported by various portions of the specification, including the description, originally-filed claims 1, 8, 15, 21 and 24, and figures 3 and 5.

Applicant is presenting new claim 60. Applicant respectfully submits that such new claim 60 is fully supported by various portions of the specification, including the description, originally-filed claims 5 and 11, and figures 2 and 4.

Applicant is presenting new claims 65 and 66. Applicant respectfully submits that such new claims 65 and 66 are fully supported by various portions of the specification, including the description, page 8, lines 2-5, and originally-filed claims 2, 6, 10, 14, 16, 19, 23, 27, 30 and 33.

Applicant is presenting new claim 67 and 68. Applicant respectfully submits that such new claims 67 and 68 are fully supported by various portions of the specification, including the description at page 5, lines 23-26, and page 7, line 25-page 8, line 7, originally-filed claims 3-4 and 28-29, and figures 6-7.

Applicant respectfully submits that such new claims 39-79 are fully supported by various portions of the specification, including the description and the figures, and the originally-filed claims. Therefore, Applicant submits that no new matter is introduced. Applicant respectfully requests consideration of and allowance of new claims 39-79.

In the Drawings

The drawings were objected to because figure 1 lacked the legend --Prior Art--. Applicant submits amended figure 1 labeled as prior art.

Further, Applicant has amended figures 2-5 to correct errors within. Applicant respectfully submits that support for the amendments are found in the specification, and do not

introduce any new matter. Detailed descriptions of each change are listed on page 2 of this response.

Accordingly, Applicant respectfully requests entry of the amendments, and withdrawal of the objection to the drawings.

Claim Objections

Claims 2, 6, 10, 14, 16, 19, 23, 27, 30 and 33 were objected to as being in improper dependent form for failing to further limit the subject matter of a previous claim. Applicant has amended these claims to overcome this objection. Applicant notes that such amendments were made to correct the improper dependent form, and not in response to a prior art rejection of the claims.

Claim 25 was objected to due to an informality. Applicant has amended this claim to overcome this objection. Applicant notes that such amendment was made to correct the informality, and not in response to a prior art rejection of the claim.

Accordingly, Applicant respectfully requests entry of the amendments, and withdrawal of these objections to the claims.

§112 Rejection of the Claims

Claims 13, 20, 26, 34 and 38 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. Applicant respectfully traverses and asserts that the claims as originally filed meet the requirements of 35 U.S.C. § 112, second paragraph. However, Applicant has amended these claims to move prosecution forward. Applicant notes that such amendments were made to correct indefiniteness, and not in response to a prior art rejection of the claims.

Applicant has amended claims 13, 20 and 26 to include a clock signal comprising a first and second edge. Applicant respectfully submits that such amendments are fully supported by various portions of the specification, including the description, and figures 2-5.

Applicant has amended claims 34 and 38 to change references of a timing signal and timing cycle to a clock signal and clock cycle, respectively. Applicant respectfully submits that such amendments are fully supported by various portions of the specification, including the summary at page 2, line 5, and the description at page 4, line 29.

Accordingly, Applicant respectfully requests entry of the amendments, and withdrawal of this rejection of the claims.

§102 Rejection of the Claims

A. Claims 1-4, 8-10 and 15-38 were rejected under 35 U.S.C. § 102(b) for anticipation by DeMone et al. (U.S. 6,266,750).

1. Claim 1, as now amended, recites,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, comprising: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals; and receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and performing a memory command in response to the received F-bit word.

(*See* claim 1.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of receiving an F-bit word comprising command and address signals in a first portion on a first edge of a clock signal and a second portion on a second edge of the clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 1. Instead, Demone et al.,

> receives streams of command packets as 4 consecutive 10-bit words on the CA[9:0] bus.

(*See* col. 4, lines 30-31.) Further, the office action states,

> As there are 10 command/address lines, there must be 10 pins.

(*See* ¶ 17.) Thus, in Demone et al. figure 3b, A0-A3 represent 4 individual words being received, each 10-bits in length, and further, being received by enough command and address pins to receive each word at each edge of the clock signal. Applicant cannot find in the cited portions of Demone et al. any disclosure, teaching, or suggestion of receiving an F-bit word in a

first portion on a first edge of a clock signal and a second portion on a second edge of a clock signal, as recited in claim 1.

Because all elements of claim 1 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 1.

2. Claim 8, as now amended, recites,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, comprising: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals; and receiving a second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and performing a memory command in response to the received F-bit word.

(*See* claim 8.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of receiving an F-bit word comprising command and address signals in a first portion on a first edge of a first cycle of a clock signal and a second portion on a first edge of a second cycle of the clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 8.

Thus, for at least the reasons stated above with respect to claim 1, and because all elements of claim 8 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 8.

3. Claim 15, as now amended, recites,

> multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word

> comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the multiple command and address pins to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a second edge of a clock signal, and wherein the memory device operates to perform a memory command in response to the received F-bit word.

(*See* claim 15.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of multiple command and address pins to receive an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different edges of a clock signal, and wherein a memory device performs a memory command in response to the completely received F-bit word, as recited in claim 15.

Thus, for at least the reasons stated above with respect to claims 1 and 8, and because all elements of claim 15 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 15.

4. Claim 18, as now amended, recites,

> multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the multiple command and address pins to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein the memory device to perform a memory command in response to the received F-bit word.

(*See* claim 18.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of multiple command and address pins to receive an F-bit word comprising a set of

command and address signals broken into two portions, each portion being received at different cycles of a clock signal, and wherein a memory device performs a memory command in response to the completely received F-bit word, as recited in claim 18.

Thus, for at least the reasons stated above with respect to claims 1, 8 and 15, and because all elements of claim 18 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 18.

5. Claim 21, as now amended, recites,

> one or more integrated circuit memory devices operable for communicating with an external controller, wherein each of the integrated circuit memory devices operates to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein each of the integrated memory circuit devices operates to receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a second edge of a clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the received F-bit word.

(*See* claim 21.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of one or more integrated circuit memory devises operable to receive an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different edges of a clock signal, and wherein each integrated circuit memory device performs a memory command in response to the completely received F-bit word, as recited in claim 21.

Thus, for at least the reasons stated above with respect to claims 1, 8, 15 and 18, and because all elements of claim 21 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant

respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 21.

6. Claim 24, as now amended, recites,

> one or more integrated circuit memory devices operable for sending and receiving signals, wherein each of the integrated circuit memory devices operates to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein each of the integrated memory circuit devices operates to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the received F-bit word.

(*See* claim 24.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of one or more integrated circuit memory devises operable to receive an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different cycles of a clock signal, and wherein each integrated circuit memory device performs a memory command in response to the completely received F-bit word, as recited in claim 24.

Thus, for at least the reasons stated above with respect to claims 1, 8, 15, 18 and 21, and because all elements of claim 24 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 24.

7. Claim 28, as now amended, recites,

> controller operates to send a word comprising command and address signals during a clock cycle of a clock signal such that the number of bits in the word sent from the controller to the integrated circuit memory device is higher than a given number of command and address pins in each integrated circuit memory device.

(*See* claim 28.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of a controller sending a word such that the number of bits in the word is higher than a given number of command and address pins in each integrated circuit memory device, as recited in claim 28. The office action states that in Demone et al.,

> there are 4 consecutive 10-bit packets that are received and then combined into a 40-bit packet; The signals of 4 packets cannot be transmitted at the same time as there are only 10 bits worth of lines and pins.

(*See* ¶ 20.) Instead, Demone et al. states that the command packets are received as 4 consecutive 10-bit words. (*See* page 4, lines 30-31.) Thus, Demone et al. is sending complete 10-bit words on 10 command and address pins. Applicant cannot find in Demone any disclosure, teaching, or suggestion of a controller sending a word such that the number of bits in the word is higher than the number of command and address pins, as recited in claim 28.

Thus, for at least the reasons stated above with respect to claims 1, 8, 15, 18, 21 and 24, and because all elements of claim 28 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 28.

8. Claim 32, as now amended, recites,

> one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises multiple command and address pins, wherein the command and address pins of each integrated circuit memory device are coupled to receive words comprising command and address signals, wherein the memory devices operate to receive words during a clock cycle of a clock signal such that the number of bits in the words sent to each integrated circuit memory device is higher than the multiple command and address pins available in each integrated circuit memory device.

(*See* claim 32.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of one or more integrated circuit memory devices coupled to receive words such that the number of bits in the words sent to each integrated circuit memory device is higher than the multiple command and address pins available in each integrated circuit memory device, as recited in claim 32.

Thus, for at least the reasons stated above with respect to claims 1, 8, 15, 18, 21, 24 and 28, and because all elements of claim 32 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 32.

9. Claim 36, as now amended, recites,

> one or more memory devices operates to receive a word comprising a number of command and address signals during more than one edge of a clock signal such that the number of bits in each word for each integrated circuit memory device are substantially higher than the predetermined number of command and address pins in each integrated circuit memory device.

(*See* claim 36.) Accordingly, Applicant cannot find in Demone et al. any disclosure, teaching, or suggestion of one or more memory devices to receive a word such that the number of bits in each words for each integrated circuit memory device are substantially higher than the predetermined number of command and address pins in each integrated circuit memory device, as recited in claim 36.

Thus, for at least the reasons stated above with respect to claims 1, 8, 15, 18, 21, 24, 28 and 32, and because all elements of claim 36 are not disclosed, taught, or suggested in Demone et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 36.

10. Regarding dependant claims 2-4, 9-10, 16-17, 19-20, 22-23, 25-27, 29-31, 33-34 and 37-38, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

B. Claims 8-10 were rejected under 35 U.S.C. § 102(b) for anticipation by Merritt (U.S. 6,192,002).

Claim 8, as now amended, recites,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, comprising: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a first subset of a set of command and address signals; and receiving a second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of command and address signals; and performing a memory command in response to the received F-bit word.

(*See* claim 8.) Accordingly, Applicant cannot find in Merritt any disclosure, teaching, or suggestion of receiving an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 8. Instead, the memory device of Merritt receives all of a first word comprising the command (activate) and a complete set of row address signals at the same time, and all of a second word comprising a separate command (block write) and a complete set of column address signals at the same time, as evidenced by 100-125 and 130, respectively, of figure 2, and figure 3.

Because all elements of claim 8 are not disclosed, taught, or suggested in Merritt, and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 8.

Regarding dependant claims 9-10, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

C. Claims 11-14 were rejected under 35 U.S.C. § 102(b) for anticipation by Ohshima et al. (U.S. 2001/0006483).

Claim 11, as now amended, recites,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, comprising: receiving a first

> portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the first portion of the F-bit word comprises G-bits, wherein G is less than F, wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; and receiving a second portion of the F-bit word substantially simultaneous with receiving a first edge of a second clock cycle of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of address signals; and performing a memory command in response to the received F-bit word.

(*See* claim 11.) Accordingly, Applicant cannot find in Ohshima et al. any disclosure, teaching, or suggestion of receiving an F-bit word comprising a set of command and address signals broken into two portions, the first portion comprising a set of command signals and a subset of the set of address signals, the second portion comprising a second subset of the set of address signals, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 11. Instead, Ohshima performs commands based upon a first fully received word comprising command signals and upper address signals, and performs separate commands based upon a second fully received word comprising lower address signals. (*See* ¶ 84.)

Because all elements of claim 11 are not disclosed, taught, or suggested in Ohshima et al., and because all elements are not shown in as complete detail as presented in the claim, Applicant respectfully submits that no *prima facie* case of anticipation presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 11.

Regarding dependant claims 12-14, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

§103 Rejection of the Claims

A. Claims 18-20 and 24-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Merritt (U.S. 6,192,002) and Ryan (U.S. 6,172,893).

1. Claim 18, as now amended, recites,

> multiple command and address pins to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the multiple command and address pins to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein the memory device to perform a memory command in response to the received F-bit word.

(*See* claim 18.) Accordingly, Applicant cannot find in Merritt or Ryan any disclosure, teaching, or suggestion of receiving an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 18. Instead, the memory device of Merritt receives all of a first word comprising the command (activate) and a complete set of row address signals at the same time, and all of a second word comprising a separate command (block write) and a complete set of column address signals at the same time, as evidenced by 100-125 and 130, respectively, of figure 2, and figure 3. Moreover, the burst command is issued upon receiving the first word containing the activate command (*see* figure 2.), further evidencing the issuance of two separate and complete words. Thus, neither Merritt nor Ryan disclose, teach, or suggest receiving an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 18.

Thus, because all elements of claim 18 are not disclosed, taught, or suggested in Merritt or Ryan, Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 18.

2. Claim 24, as now amended, recites,

> one or more integrated circuit memory devices operable for sending and receiving signals, wherein each of the integrated circuit memory devices operates to receive a first portion of an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, wherein the first portion of the F-bit word comprises a first subset of the set of command and address signals, wherein the multiple command and address pins receive the first portion of the F-bit word substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein each of the integrated memory circuit devices operates to further receive a second portion of an F-bit word, wherein the second portion of the F-bit word comprises a second subset of the set of command and address signals, wherein the multiple command and address pins receive the second portion of the F-bit word substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the received F-bit word.

(*See* claim 24.) Accordingly, Applicant cannot find in Merritt or Ryan any disclosure, teaching, or suggestion of receiving an F-bit word comprising a set of command and address signals broken into two portions, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 24.

Thus, for at least the reasons stated above with respect to claim 18, and because all elements of claim 24 are not disclosed, taught, or suggested in Merritt or Ryan, Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 24.

3. Regarding dependant claims 19-20 and 25-27, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

B. Claims 5-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohshima et al. (U.S. 2001/0006483) and Pawlowski (U.S. 5,973,989).

Claim 5, as now amended, recites,

> receiving an F-bit word, wherein F is a positive integer, wherein the F-bit word comprises a set of command and address signals, comprising: receiving a first portion of the F-bit word substantially simultaneous with receiving a first edge of a clock signal, wherein the first portion of the F-bit word comprises G-bits,

> wherein G is less than F, wherein the G-bit portion comprises a set of command signals and a first subset of a set of address signals; and receiving a second portion of the F-bit word substantially simultaneous with receiving a second edge of the clock signal, wherein the second portion of the F-bit word comprises H-bits, wherein H is F-G, wherein the H-bit portion comprises a second subset of the set of address signals; and performing a memory command in response to the received F-bit word.

(*See* claim 5.) Accordingly, Applicant cannot find in Ohshima et al. or Pawlowski any disclosure, teaching, or suggestion of receiving an F-bit word comprising a set of command and address signals broken into two portions, the first portion comprising a set of command signals and a subset of the set of address signals, the second portion comprising a second subset of the set of address signals, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 5. Instead, Ohshima et al. performs commands based upon a first fully received word comprising command signals and upper address signals, and performs separate commands based upon a second fully received word comprising lower address signals. (*See* ¶ 84.) Thus, neither Ohshima et al. nor Pawlowski disclose, teach, or suggest receiving an F-bit word comprising a set of command and address signals broken into two portions, the first portion comprising a set of command signals and a subset of the set of address signals, the second portion comprising a second subset of the set of address signals, each portion being received at different cycles of a clock signal, and performing a memory command in response to the completely received F-bit word, as recited in claim 5.

Thus, because all elements of claim 5 are not disclosed, taught, or suggested in Ohshima et al. or Pawlowski, Applicant respectfully submits that no *prima facie* case of obviousness presently exists with respect to this claim. Accordingly, Applicant respectfully requests withdrawal of this rejection of claim 5.

Regarding dependant claims 6-7, Applicant respectfully submits that such claims include patentable subject matter beyond that recited in their respective base claims, and Applicant reserves the right to later present further remarks concerning such dependent claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 28 June '06 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28 day of June, 2006.

Name _____ Signature _____